



# MSc Distance Learning Prospectus 2009/10



University  
of Glasgow



***Building Electronic Design Skills***

*March 2010*



## Institute for System Level Integration

In response to demand from industry for flexible and accessible courses, iSLI offers a set of modules by distance learning in the field of System Level Integration. It is designed to give electronic engineers a competitive edge by enabling them to build their skills in a discipline of importance to the semiconductor industry and better prepare them to take advantage of the impending market upswing. It will also fulfil one of the key missions of iSLI to address the global shortage of skilled electronic design engineers.

**Our programme can only be studied as CPD modules.**

### Course Delivery

Modules are available online and students can access course materials at any hour of the day. Dedicated tutors will support students by email or other methods, including web-based discussion groups, post and telephone. Students are assessed by a combination of exams and coursework.

Taster courses may be previewed at <http://www.sli-institute.ac.uk/moodle/>.

We advise that a maximum of two modules be studied concurrently. The typical duration of a module is four months and students are expected to finish the module within 13 months after which access to the material is blocked and considered completed or withdrawn.

### Syllabus

Introduction to Hardware Design Automation  
Introduction to Embedded Software Engineering

Embedded Operating Systems  
System Level Integration  
IP Block Integration  
System Partitioning  
VLSI Design

Sensor Networks  
Embedded Networking

Microcontrollers and Microprocessors

Introduction to Verification

### Interested?

To be kept up-to-date with the development of the DL programme and notified of module start dates, please email or call:

**MSc/Distance Learning Office**  
**Institute for System Level Integration**  
**Heriot-Watt University Research Park**  
**Research Avenue North**  
**Edinburgh**  
**EH14 4AP**

**Email: [distlearn@sli-institute.ac.uk](mailto:distlearn@sli-institute.ac.uk)**  
**Tel: +44 (0) 131 510 0673**  
**Fax: +44 (0) 131 449 3141**



### **Introduction to Hardware Design Automation**

**(8 credits)**

Enables students to be able to appreciate the basic aims and limitations of an HDL. Shows how to use Verilog to code and test basic combining circuits and sequential clocked circuits such as counters and Finite State Machines. This module is also designed to make students aware of some of the basic constructs of VHDL and how they compare with those in Verilog. This module is a pre-requisite for the hardware based modules. **(Page 4)**

### **Introduction to Embedded Software Engineering**

**(8 credits)**

Introduces students to the basic concepts, syntax and structure of the C programming language with relation to embedded software systems. This module is a pre-requisite for the software based modules. **(Page 5)**

### **Embedded Operating Systems**

**(15 credits)**

This module covers the general embedded software engineering process and some of the specific considerations due to complex IC engineering. Understanding the fundamental elements of real-time embedded operating systems and applying RTOS techniques in a practical manner. **(Page 7)**

### **System Level Integration**

**(15 credits)**

Presents the principles of design re-use in the context of system on chip technology. The design and selection of soft, firm and hard IP blocks are considered. Emerging design practices and standards are reviewed. Two target technologies are addressed: deep-submicron ASICs and field programmable gate arrays. **(Page 8)**

### **IP Block Integration**

**(15 credits)**

Provides an appreciation of the design issues involved in assembling a system-level design from pre-defined and pre-characterised hardware/firmware/software IP blocks. Discusses how system-level designs can be verified and tested, introducing the latest technologies and practices. Includes dynamic verification, static verification and Design-for-Test techniques. Focus is placed on achieving more rapid design turnaround times in the face of ever-increasing chip complexities. **(Page 9)**

### **System Partitioning**

**(15 credits)**

Provides an in-depth understanding of the methodology of the design of complex digital systems that comprises both hardware and software. The methodology begins with requirements capture and proceeds through executable functional modelling, architectural exploration by partitioning into functional blocks and mapping onto physical hardware such as systems-on-chip. **(Page 10)**

### **VLSI Design**

**(15 credits)**

Provides a top-down understanding of VLSI Design principles, starting from algorithmic design synthesis, proceeding through gate and transistor levels down to layout. Emphasis is made at various levels on high performance design in terms of speed, power and area. **(Page 11)**



### Sensor Networks

(8 credits)

Explores some of the more advanced operating system concepts required to build sensor network systems. (Page 12)

### Embedded Networking

(8 credits)

This module covers some of the more advanced concepts used in embedded systems software, in particular, the use of networking, network applications, and distributed systems technologies. (Page 13)

### Microcontrollers and Microprocessors

(15 credits)

Introduces the architectural building blocks of modern microcontrollers and microprocessors, their bus, interconnect architectures, memory hierarchies, and metrics for performance determination and comparison. Differences between processors and controllers are highlighted, and issues relating to the use of processor/controller cores within embedded and System-on-Chip applications are emphasised. (Page 14)

### Introduction to Verification

(15 credits)

Provides a good basic knowledge of VLSI functional verification, methodologies, allowing participants to become useful members of a verification team. The emphasis in this module is on the practical aspects of the planning and execution of functional verification of complex digital ASIC/FPGA designs. (Page 16)

The modules "Introduction to Hardware Design Automation" and "Introduction to Embedded Software Engineering" are at undergraduate level and do not count towards the MSc in System Level Integration.

## Fees

### International Students

15 credit module	£1,200
8 credit module	£ 600

The course fee covers access to learning materials, tutor support and examination fees. It does not cover internet access costs, travel and accommodation for any residential element of the course, or (optional) graduation fees.

Fees are payable in advance. Students will not be enrolled until iSLI has received payment.



## Timetable

The timetable below shows the standard start and end date (examination month) for each of our modules. Please contact the iSLI to confirm dates and your specific requirements.

<b>Module</b>	<b>Start Date</b>	<b>Finish Date</b>
Introduction to Hardware Design Automation	Spring	September
Introduction to Embedded Software Engineering	Spring	September
Embedded Operating Systems	Summer	January
System Level Integration	Summer	January
IP Block Integration	Autumn	April
System Partitioning	Autumn	April
VLSI Design	Summer	January
Sensor Networks	Autumn	April
Embedded Networking	Autumn	April
Microcontrollers and Microprocessors	Autumn	April
Introduction to Verification	Summer	January



## Introduction to Hardware Design Automation

**Module Credits:** 8  
**Learning Hours:** 80

**Module Convenor:**  
**Tutor:**

### Module Aims

The aim of this module is for students to be able to appreciate the basic aims and limitations of an HDL, and be able to use Verilog to code and test basic combining circuits and sequential clocked circuits such as counters and Finite State Machines. This module is also designed to make students aware of some of the basic constructs of VHDL and how they compare with those in Verilog.

### Learning Objectives

After successful completion of this module a student will:

- be aware of the need for, and the concepts behind hardware description languages ;
- be familiar with Verilog simulators – at first a simple PC version and then, during the optional residential day, with Cadence Verilog;
- be able to code combinatorial and sequential logic into Verilog;
- be able to code simple finite state machines into Verilog;
- have been exposed to the basic structures of VHDL, and be aware of the key differences between Verilog and VHDL.

### Background to the Module

Introduction to Hardware Design Automation is a Verilog primer course. It is not a course in digital design and purely aims to introduce the concepts and structures of Verilog. This module should be

seen as an introductory course that prepares students for other compulsory iSLI modules.

### Prerequisite Knowledge

Students should possess a basic digital design knowledge found in a typical electronics or computer science undergraduate degree course.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials.

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

To register for the module contact:

**MSc/Distance Learning Office**  
**Institute for System Level Integration**  
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## Introduction to Embedded Software Engineering

**Module Credits:** 8  
**Learning Hours:** 80

**Module Convenor:** Andrew Colin  
**Tutor:** Andrew Colin

### Module Aims

To introduce students to the basic concepts, syntax and structure of the C programming language with relation to embedded software systems.

### Learning Objectives

After successful completion of this module a student will:

- have a working knowledge of the syntax and capabilities of the C language;
- be able to write C programs;
- understand the significance of C programs in the design of embedded systems.

### Background to the Module

This module is a software primer course and should be seen as an introductory course that prepares students for other iSLI embedded software modules.

### Prerequisite Knowledge

Basic programming skills would be useful though not essential.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials.

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

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## Embedded Operating Systems

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenors:** Prof Joe Sventek  
**Tutor:**

### Module Aims

The aim of this module is to introduce the student to the general embedded software engineering process and some of the specific considerations created by system on chip engineering. The study material and presentations are supported by practical C programming exercises using GNU tools in the Unix environment. Whilst studying this module, students may also be given web access to online tools for SoC simulation exercises.

### Learning Objectives

After successful completion of this module a student will:

- understand the principles of hardware/software integration at the lowest embedded level;
- comprehend hardware/software data manipulation (such as DSP) restrictions;
- understand the methods available for parallel software implementation using virtual/simulation target systems;
- understand the components of the embedded software implementation tool chain, including compilation, build, test and debug resources.

### Background to the Module

The area of system on chip is, in many respects, primarily a hardware and software integration problem as the majority of these SoC devices will have some form of microprocessor or microcontroller core included. It is therefore central that SoC hardware engineers are proficient in software implantations issues and

that embedded software engineers developing for a SoC target have an awareness of the hardware architecture specifics of SoC devices.

### Prerequisite Knowledge

iSLI Module 'Introduction to Embedded Software Engineering' and/or reasonable proficiency in C programming with some experience as a Unix user.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials.

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

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## System Level Integration

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenor:** Prof Tughrul Arslan  
**Tutors:** Prof Tughrul Arslan  
Dr Ahmet Erdogan

### Module Aims

The aim of this module is to present the principles of design re-use in the context of system on chip technology. The design and selection of soft, firm and hard IP blocks are considered. Emerging design practices and standards are reviewed. Two target technologies are addressed: deep-submicron ASICs and field programmable gate arrays.

### Learning Objectives

After successful completion of this module a student will:

- understand the technological conditions behind the need for greater design re-use for SoC;
- be able to differentiate between the different types of intellectual property blocks, their advantages and disadvantages;
- be able to evaluate the appropriateness of a particular IP block for a given application;
- be able to assess a piece of soft IP using the OpenMore guidelines;
- be able to apply the design guidelines for IP block authoring;
- understand the effects of DSM technology on the CAD flow for ASIC design;
- be familiar with the DSM ASIC design methodology.

### Industrial Prospective

- Industrial case study 1: IP Reuse for FPGAs – Xilinx;
- Industrial Case Study 2: IP Trading: Integration, Marketing and Legal Issues.

### Background to the Module

This module forms part of the iSLI compulsory curriculum.

### Prerequisite Knowledge

Knowledge of a hardware description language. Before commencing this module, students are advised to have studied iSLI module 'Introduction to Hardware Design Automation'.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials. (Where students do not have a broadband internet connection, it may be necessary to attend iSLI or a partner organisation for access to design tools).

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

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## IP Block Integration

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenor:** Dr Paul Jackson  
**Tutor:** Dr Paul Jackson

### Module Aims

The aim of the module is to provide an appreciation of the design issues involved in assembling a system-level design from pre-defined and pre-characterised hardware/firmware/software IP blocks. The module discusses how system-level designs can be verified and tested, introducing the latest technologies and practices and includes dynamic verification, static verification and Design-for-Test techniques. The focus is placed on achieving more rapid design turnaround times in the face of ever-increasing chip complexities.

### Learning Objectives

After successful completion of this module, the student will be able to:

- identify and discuss the major issues that have to be addressed when assembling a system-level design;
- describe when it is appropriate to adopt a platform-based approach, and discuss current examples;
- show knowledge of design-for-test techniques, and be able to describe their appropriate deployment in core-based manufacturing test of system-level designs;
- describe and compare simulation technologies;
- explain approaches to developing simulation testbenches, and discuss the kinds of evidence they give about a design's correctness;
- discuss the merits of cutting-edge verification tools such as equivalence checkers, static timing analysers, and testbench automation tools, and demonstrate basic familiarity with examples of these tools.

### Background to the Module

The era of deep submicron technology allows system-on-chip (SoC) designers to build chips of

tens of millions of transistors. Design, verification and test methods are being re-examined to find ways to handle this complexity. The re-use and integration of pre-designed and pre-verified IP blocks is a cornerstone of new approaches.

### Prerequisite Knowledge

Material covered in iSLI Modules 'IP Block Authoring' and 'VLSI Design' and reasonable proficiency with VHDL or Verilog HDL. Some familiarity with object-oriented programming (eg. C++ or Java) is preferred.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials. (Where students do not have a broadband internet connection, it may be necessary to attend iSLI or a partner organisation for access to design tools).

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

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### Registration

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## System Partitioning

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenor:** Dr Fernando Rodriguez  
**Tutor:** Dr Fernando Rodriguez

### Module Aims

To provide an in-depth understanding of the methodology of the design of complex digital systems that comprises both hardware and software. The methodology begins with requirements capture and proceeds through executable functional modelling, architectural exploration by partitioning into functional blocks and mapping onto physical hardware such as SoC.

### Learning Objectives

After successful completion of this module a student will be able to:

- appreciate the need for an integrated design process from system level design through to silicon;
- understand the use of UML as a modeling language;
- appreciate language requirements and the current capabilities of languages for system level design;
- appreciate scheduling and communication issues;
- understand the objectives and activities of the system partitioning process;
- capture a specification and implement it as a functional model in the SpecC language;
- carry out architectural exploration and have an appreciation of the need for and means of performance estimation of architectural models;
- create testbenches and carry out timing analysis using SpecC;
- understand the concept of orthogonality between functional and communications models and be able to carry out bus allocation,

channel partitioning and protocol insertion in communications models.

### Prerequisite Knowledge

Familiarity with basic electronic circuits and an appreciation of the importance of computer aided design in circuit and system synthesis; an understanding of introductory level logic and digital systems; and sound knowledge of at least one high level programming language, including dynamic data structures involving pointers or references (C, C++ Pascal, Ada, Java, etc.).

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials.

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

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## VLSI Design

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenor:** Prof Tughrul Arslan  
**Tutors:** Prof Tughrul Arslan  
Dr Ahmet Erdogan

### Module Aims

The aim of this module is to provide a top-down understanding of VLSI Design principles, starting from algorithmic design synthesis, proceeding through gate and transistor levels down to layout. Emphasis is made at various levels on high performance design in terms of speed, power and area.

### Learning Objectives

After successful completion of this module a student will:

- have knowledge of architectural design and synthesis principles;
- understand the main synthesis and optimisation techniques employed during the design of high performance VLSI systems;
- comprehend the role and the main components of modern VLSI CAD tools;
- understand the synthesis and optimisation techniques employed during the design of high performance VLSI systems;
- understand the need for various simulation techniques and their use during the design of complex VLSI systems;
- be able to perform design trade-offs at various stages of the design synthesis process for parameters such as speed, power and area;
- appreciate the impact of CMOS transistor level and logic design of primitive gates, key logic and arithmetic components, multiplexers, shifters and adders on performance;
- comprehend layouts of VLSI designs at floor planning level, down through the hierarchy to transistor level;
- be familiar with the content and design of standard cell libraries including AOI and several other design styles;
- be familiar with types of latches and the distinction between D-flip-flops and implicit state devices;

- be able to describe the effects of delay and clock distribution on synchronous systems and solutions such as true single phase clocking and NORA logic.

### Background to the Module

This module is one of iSLI's compulsory modules in SoC Design.

### Prerequisite Knowledge

Basic digital design and circuit design such as that found in a typical Electronics or Computer Science undergraduate degree course. For students with no HDL experience, 'Introduction to Hardware Design Automation' is recommended as a pre-requisite for Units 7-12: High level and architectural design.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials. (Where students do not have a broadband internet connection, it may be necessary to attend ISLI or a partner organisation for access to design tools).

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

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## Sensor Networks

**Module Credits:** 8  
**Learning Hours:** 80

**Module Convenor:** Prof Joe Sventek  
**Tutor:** Dr Wim Vanderbauwhede

### Module Aims

The aim of this module is to explore some of the more advanced operating system concepts required to build sensor network systems. The exploration will take place in the context of the Tiny\* software and mote hardware produced by the Berkeley team. The study material and presentations are supported by practical programming exercises.

### Learning Objectives

On completion of this module students will be able to:

- Understand how to design, simulate, and implement applications using TinyOS targeted at mote hardware;
- Understand how to query information from a Tiny network;
- Understand how Maté enables the construction of virtual machines (middleware) to facilitate sensor network construction;
- Understand how encryption can be provided in such networks.

### Syllabus Content

- TinyOS fundamentals;
- TOSSIM – TinyOS mote simulator;
- Maté – a virtual machine for TinyOS motes;
- TinyDB – a query processing system for extracting information from a network of TinyOS sensors;
- TinySEC – link layer encryption for tiny devices design, simulation, and implementation of a sample application.

### Prerequisite Knowledge

iSLI module 'Introduction to Embedded Software Engineering' and/or reasonable proficiency in C (or C++) programming with some experience as a Unix user. Embedded Operating Systems. Embedded Networking (ideal taken concurrently).

### Format

The module is delivered by online distance learning. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials. (Where students do not have a broadband internet connection, it may be necessary to attend iSLI or a partner organisation for access to design tools).

### Assessment

The module is assessed by 100% coursework.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

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## Embedded Networking

**Module Credits:** 8  
**Learning Hours:** 80

**Module Convenor:** Prof Joe Sventek  
**Tutor:**

### Module Aims

The aim of this module is to introduce some of the more advanced concepts used in embedded systems software, in particular, the use of networking, network applications, and distributed systems technologies. The study material and presentations are supported by practical programming exercises.

### Learning Objectives

On completion of the module students will be able to:

- Understand TCP/IP internetworking and standard internet socket programming;
- Understand Internet application protocols and the extensible markup language (XML);
- Understand different application interaction styles;
- Create embedded application software in the various styles.

### Background to the Module

Current embedded system trends are towards network enabled devices and the majority of current and future system on chip devices will be used within a networked environment. In particular, internet technologies are becoming the predominant form of networking for embedded systems due to the inherent interoperability with general information technology infrastructures. In order to create these internet-enabled embedded system applications, it is necessary to understand technologies and standards such as the TCP/IP protocol suite and internet applications such as HTML, XML, HTTP, SMTP, etc. This module introduces the most common internet standards and technologies and its practical use with the

VxWorks real-time operating system. A single session introducing defensive and reusable programming concepts is also included.

### Prerequisite Knowledge

Embedded Operating Systems module.  
Advanced proficiency in C programming, with some experience as a UNIX user.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials. (Where students do not have a broadband internet connection, it may be necessary to attend iSLI or a partner organisation for access to design tools).

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

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## Microcontrollers and Microprocessors

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenor:** Dr James Herd  
**Tutor:** Dr Vijayanand Najarajan

### Module Aims

To introduce the architectural building blocks of modern microcontrollers and microprocessors, their bus, interconnect architectures, memory hierarchies, and metrics for performance determination and comparison. Differences between processors and controllers are highlighted, and issues relating to the use of processor/controller cores within embedded and System-on-Chip applications are emphasised.

### Learning Objectives

After successful completion of this module a student will:

- understand the main architectural blocks within a processor/controller and their relationship to each other;
- be able to describe the different performance metrics available and be able to calculate, using these, the relative benefits of different devices/architectures;
- understand the bus, interconnect and memory hierarchies attached to processor/controller chips/cores;
- be familiar with the principles and concepts of virtual memory systems and understand the associated hardware acceleration techniques used within processors;
- understand the reasons and benefits behind the move from CISC to RISC processor/controller architectures and the associated instruction set changes;
- be able to describe many of the advanced acceleration techniques utilised in modern processors/controllers to enhance performance;
- understand the issues relating to the use of processor/controller cores in System-on-Chip applications.

### Background to the Module

This module introduces students to the various architectural, performance and implementation issues in modern microcontrollers and microprocessors. Previous knowledge of processor architectures is not required as the module starts at ground level and builds up to the more advanced modern techniques.

### Prerequisite Knowledge

No specific previous knowledge of, or training in, microcontrollers or microprocessors is assumed. A general, basic knowledge of computer systems would be helpful, though not essential.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course.

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

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## Introduction to Verification

**Module Credits:** 15  
**Learning Hours:** 150

**Module Convenor:** Dr Paul Jackson  
**Tutor:** Dr Paul Jackson

### Module Aims

The aim of this module is to provide students with a good basic knowledge of VLSI functional verification, methodologies, allowing them to become useful members of a verification team. The emphasis in this module is on the practical aspects of the planning and execution of functional verification of complex digital ASIC/FPGA designs.

### Learning Objectives

After successful completion of this module a student will:

- have a basic understanding of the scope, need, limitations and terminology in VLSI verification;
- have a basic understanding of Formal Verification and where it currently fits into the VLSI verification flow;
- know how to approach verification planning;
- have a basic understanding of how to manage verification, using functional coverage, issue tracking and common sense;
- have experience (using an ARM AMBA based case-study example), of how verification of a processor-based System-on-Chip (SoC) was achieved;
- have performed some basic verification tasks.

### Background to the Module

This module is available as part of the iSLI curriculum, providing a basic understanding of one of the major bottlenecks in VLSI design today: verification.

'Introduction to Hardware Design Automation' and 'VLSI Design'. Students should have a reasonable level of EDA knowledge - gained from attending relevant iSLI MSc module(s). A reasonable level of Verilog knowledge is also required to complete practical exercises.

### Format

The module is delivered by online distance learning in conjunction with a ½ day exam. Students will access the iSLI Moodle e-learning portal for the online part of the course and hands on practical sessions and tutorials. (Where students do not have a broadband internet connection, it may be necessary to attend iSLI or a partner organisation for access to design tools).

### Assessment

The module is assessed by 40% coursework and 60% examination.

### Cost

Please refer to fees section on page 3.

### Start Date

Contact iSLI for details.

### Registration

To register for the module contact:

**MSc/Distance Learning Office**  
**Institute for System Level Integration**  
**Heriot-Watt University Research Park**  
**Research Avenue North**  
**Edinburgh**  
**EH14 4AP**

**Email:** [distlearn@sl-i-institute.ac.uk](mailto:distlearn@sl-i-institute.ac.uk)

**Tel:** +44 (0) 131 510 0673

**Fax:** +44 (0) 131 449 3141

### Prerequisite Knowledge



## Disclaimer

This prospectus was revised in March 2010 and every care has been taken to ensure that the information contained in it is accurate at the time of printing. However, the course programme described is subject to continuing development and changed circumstances may necessitate cancellation or alteration to the programme, fees and other matters.

The Institute reserves the right to make variations to the programme or other matters if such action is considered necessary at any time before or after a student's admission to the course. In such circumstances the Institute will take all reasonable steps to minimise any resultant disruption and give as much notice as possible of any such changes. Please note that the Institute does not accept any liability arising out of or in connection with any such changes.