

Techniques for Designing testable Boards and Systems Based on Boundary-Scan Technology

Title

Techniques for Designing testable Boards and Systems Based on Boundary-Scan Technology

Presenter

Eric Cormack
DFT Solutions Ltd

Date and Venue

7-9 July 2009
iSLI, Livingston

Cost

£1,050 per person + VAT
(Discounts available please enquire)

Mentor Graphics Passbook = 3 Tokens per person

Contact

If you have any course queries, please contact Suzanne O'Hare on 01506 469303 or by emailing suzanne.ohare@sl-i-institute.ac.uk.

Course Aims

The course aims to motivate chip and board designers to consider life-cycle test needs as an integral part of a product design process to the point where they proactively design in testability.

The course will also identify the life-cycle needs of a product in respect of test; to present the basics of the IEEE 1149.1 Boundary Scan Standard; to identify the synergy of boundary scan, BIST and internal scan at system integration and field service levels of test using 1149.1 as a backplane bus.

Who Should Attend?

Digital board/system and field service designers, test engineers, project managers and product support engineers

Course Content

Day 1—An introduction To The 1149.1 Boundary Scan Standard: Chip-Level Architecture and Board-Level Application, IEEE 1532 In-System Configuration Standard.

Topics covered include:

- the basic chip-level architecture and Boundary-Scan Description Language (BSDL) with emphasis on the use and benefits at board level, concentrating on pattern generation for detection and diagnosis of faults within the boundary scan domain.
- handling faults outside the domain (cluster and memory-array tests)
- introduction to the IEEE 1532 In-System Configuration Standard leveraging 1149.1 structures to enable programming of CPLDs and FPGAs in situ on the board.

Day 2—Chip and Board DFT Guidelines, Board DFT Case Study, IEEE 1149.6 “AC-EXTEST” Standard for AC-Coupled LVDS Interconnects

Topics covered include:

- comprehensive set of practical chip and board DFT guidelines, based on maximizing the use of on-board boundary-scan devices
- introduces a systematic way of reviewing a board’s testability, illustrated by a real-life case study. The special problem of dealing with configured or un-configured FPGAs is discussed in depth with relation to one of today’s more complex FPGAs – the Xilinx Virtex-2 Pro and the more recent Virtex 4 and Virtex 5 devices.
- The IEEE 1149.6 “AC-EXTEST” Standard, applied to the testing of high-speed AC-coupled low-voltage differential signal buses, is also discussed, together with other ways of testing High-Speed Serial IO buses such as loopback test and the use of Interconnect BIST engines (IBIST).

Day 3—Applications of Boundary Scan to System And Field-Service Test, Additional Board Test/DFT Topics, Quizzes.

Topics covered include:

- an introduction to the various styles of electrical board test (In-Circuit Test and its Manufacturing Defect Analyser and Flying Probe Test variants)
- non-electrical board test (Automated Optical Inspection and Automated X-Ray Inspection).
- IEEE 1149.4, targeted at mixed-signal devices
- IP security in an 1149.1-enabled device.
- the impact on board test of the move to lead-free solder.
- creating BSDL files for System-in-Packages.
- In addition, there are a variety of live quizzes on the various Standards

Presenter

Eric has over 30 years of experience in the field of design-for-test. He has implemented a wide range of DfT solutions in IC, board, Soc and MCM level test. Eric started his career working with military applications for the UK MoD, implementing customised board level design-for-test solutions. He moved on from there to establish a test services company in the USA for his UK based company

providing a wide range of services from DfT consultancy in customer designs to full turn-key packages, delivering tester hardware and test program suites in ICT and Functional Test for a variety of ATE platforms. Eric has implemented custom scan and BIST based solutions at IC level, boundary scan at IC, SoC and board level, and has developed customised test and diagnostic solutions for MCM applications in satellite systems. Eric has over 12 years experience in the semiconductor industry working for Hitachi and Philips/NXP.

Fees

Fees cover tuition, course notes, lunches and light refreshments.

Accommodation

Information on local hotels is available from Amanda Connelly amanda.connelly@sli-institute.ac.uk.

Cancellations

A 10% administration fee is levied for cancellations made up to two weeks prior to the start of the course. Cancellations thereafter will be liable to the loss of the full fee. Substitutions may be made at any time up until the start of the course.

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Cancellations made up to two weeks prior to the start of the course will result in a 1 token per booked place charge. Cancellations thereafter will be liable for full token fees. Substitutions may be made at any time up until the start of the course.

The Institute reserves the right to cancel an advertised course at short notice or to postpone or make such alterations to the content of a course as may be necessary. If a course is cancelled, fees will be refunded in full.